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LINDA E. HASTINGS

Any fee due as a result of this paper, not covered by an enclosed check, may be charged on Deposit Acct. No. 50-1290.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor:

Eiki HASHIMOTO

Serial No.:

10/015,209

Filed:

November 16, 2001

Title:

SEMICONDUCTOR CIRCUIT DESIGNING APPARATUS AND A SEMICONDUCTOR CIRCUIT DESIGNING METHOD IN WHICH THE NUMBER OF STEPS IN A CIRCUIT DESIGN

AND A LAYOUT DESIGN IS REDUCED

Examiner:

Annette M. Thompson

Group Art Unit:

2825

Commissioner for Patents P. O. Box 1450 Alexandria, VA 22313-1450

RESPONSE TO OFFICE ACTION

SIR:

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In response to the Office Action mailed on October 8, 2004, the period for responding thereto having been set to expire after January 8, 2005, please consider the following remarks: